Semiconductor Integrated Circuit, Logic Operation Circuit, and Flip Flop

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of priority under 35USC § 119 to Japanese Patent Application No. 2000-184398, filed on June 20, 2000, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

(i) Field of the Invention

The present invention relates to a semiconductor integrated circuit constituted by combining a plurality of transistors, a logic operation circuit, and a flip flop, and more particularly to a technique for reducing consumption power and improving a signal transmission rate.

(ii) Description of the Related Art

In order to increase the speed of a CMOS logic circuit, the circuit must be constituted by transistors with a low threshold voltage. However, when the threshold voltage of the transistors lowers, a leak electric current increases at the time of standby. To avoid this problem, there is proposed an MT (Multiple Threshold voltage)-CMOS circuit which can simultaneously achieve the high-speed operation of the circuit and the low leak electric current at the time of standby.

FIG. 9 is a conventional circuit diagram of the MT-CMOS circuit. The circuit shown in FIG. 9 includes a Low-Vth block 1 which is connected between a virtual power supply line VDD1 and a virtual ground line VSS1 and constituted by a plurality of transistors having a low threshold voltage, a transistor Q1 which is connected between the virtual power supply line VDD1 and a power supply line VDD and has a high threshold voltage, and a transistor Q2 which is connected between the virtual ground line VSS1 and a ground line VSS and has a low threshold voltage.

In the operation (active), the both transistors Q1 and Q2 are turned on, and a power supply voltage is supplied to the Low-Vth block 1. Since the Low-Vth block 1 is constituted by a

transistor having a low threshold voltage, it operates at a high speed.

On the other hand, in the standby mode, the both transistors Q1 and Q2 are turned off, and a leak path extending from the power supply line to the ground line is shut off, thereby reducing the leak electric current.

However, since the ON resistance exists in the transistors Q1 and Q2 illustrated in Fig. 9, the potential of the virtual power supply line and the virtual ground line tends to be unstable in active state, and the circuit operation of the entire Low-Vth block 1 also becomes unstable.

Further, when the Low-Vth block 1 is active, since the leak electric current flows from the power supply line to the ground line through the leak path, it is difficult to reduce the leak electric current in this period. Furthermore, since a transistor having a high threshold voltage must be added besides the Low-Vth block 1, a circuit area increases, and data held in a flip flop or a latch in the Low-Vth block 1 is disadvantageously lost in the standby mode.

On the other hand, in order to minimize these problems, there is proposed such a circuit as shown in FIG. 10 in which only some cells in the logic circuit are replaced with transistors having a low threshold voltage. A heavy line in FIG. 10 indicates a cell constituted by using transistors having a low threshold voltage.

However, when each of some cells is constituted by transistors having a low threshold voltage as shown in FIG. 10, since the leak electric current flows to this cell, it is impossible to satisfy a demand to reduce the consumption power as much as possible in the standby mode (waiting period) as in a mobile phone and the like.

SUMMARY OF THE INVENTION

In view of the above-described problems, it is an object of the present invention to provide a semiconductor integrated circuit, a logic operation circuit and a flip flop capable of performing high-speed operation and have a leak electric current

reduced.

To achieve this object, according to the present invention, there is provided a semiconductor integrated circuit comprising: a plurality of gate circuits; and a control circuit configured to control the operation of some gate circuits among the plurality of gate circuits, each of some gate circuits among the plurality of gate circuits including: a logic circuit constituted by a plurality of first transistors; and a switch circuit which can switch whether a power supply voltage is supplied to the logic circuit, is constituted by a second transistor having a threshold voltage higher than that of the first transistor, and is controlled by the control circuit.

According to the present invention, since only some gate circuits in the semiconductor integrated circuit are constituted by using transistors having a low threshold voltage, the speed of, e.g., only a part that accurate timing is required can be increased by using the transistors having a low threshold voltage, and any other part can be constituted by using the transistors having a reduced leak electric current and a high threshold voltage. As a result, both increase in speed and reduction in consumption power can be achieved.

Moreover, all the gate circuits in the semiconductor integrated circuit are constituted by transistors having a high threshold voltage and a low threshold voltage in the conventional MT-CMOS circuit, whereas only part of the gate circuits (for example, only a gate circuit on a critical path) is constituted by transistors having a high threshold voltage and a low threshold voltage in the present invention. Therefore, a device forming area of the circuit can be reduced as compared with the prior art MT-CMOS circuit, thereby attaining high integration.

In addition, according to the present invention, there is provided a logic operation circuit comprising: a gate circuit constituted by a plurality of first transistors; and a second transistor which is connected between a second reference voltage line and the virtual voltage line and has a threshold voltage higher than that of the first transistor, a source/drain terminal of the first transistor in the gate circuit being connected to

either a source/drain terminal of another first transistor in the gate circuit or an output terminal of the gate circuit.

Additionally, according to the present invention, there is provided a logic operation circuit comprising: a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors; and a second transistor which is connected between the virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of the first transistor; and a third transistor which is connected between the first reference voltage line and an output terminal of the gate circuit and has a threshold voltage higher than that of the first transistor, the second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa.

Further, according to the present invention, there is provided a logic operation circuit comprising: a gate circuit constituted by a plurality of first transistors and connected to first and second virtual voltage lines; a second transistor which is connected between a first reference voltage line and the first virtual voltage line and has a threshold voltage higher than that of the first transistor; a third transistor which is connected between a second reference voltage line and the second virtual voltage line and has a threshold voltage higher than that of the first transistor; and a storage circuit capable of holding output logic of the gate circuit, the second and the third transistors being controlled to be OFF when the storage circuit holds the output logic of the gate circuit, and the second and third transistors being controlled to be ON when the storage circuit does not hold the output logic of the gate circuit.

Furthermore, according to the present invention, there is provided a logic operation circuit comprising: a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines; a second transistor which is connected between a first reference voltage line and the first virtual voltage line and has a threshold voltage higher than that of the first transistor; a third transistor which

is connected between a second reference voltage line and the second virtual voltage line and has a threshold voltage higher than that of the first transistor, and a bypass circuit which is connected to the gate circuit in parallel and constituted by a circuit which is substantially equal to the gate circuit by using a plurality of fourth transistors having a threshold voltage higher than that of the first transistor, the bypass circuit being connected between the first and second reference voltage lines.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram showing a first embodiment of a semiconductor integrated circuit according to the present invention;

FIG. 2 is a conventional circuit diagram corresponding to the circuit illustrated in FIG. 1;

FIG. 3 is a circuit diagram showing a first concrete example of an MT gate cell constituting a gate circuit 1 depicted in FIG. 1;

FIG. 4 is a circuit diagram showing a second concrete example of the MT gate cell;

FIG. 5 is a circuit diagram showing a third concrete example of the MT gate cell;

FIG. 6 is a circuit diagram showing a fourth concrete example of the MT gate cell;

FIG. 7A is a symbol diagram showing a composite gate having no intermediate node, and FIG. 7B is an internal circuit diagram of FIG. 7A;

FIG. 8 is a circuit diagram showing a second embodiment of a semiconductor integrated circuit according to the present invention;

FIG. 9 is a conventional circuit diagram of an MT-CMOS circuit; and

FIG. 10 is a conventional circuit diagram in which only some cells in a logic circuit are replaced with transistors having a low threshold voltage.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor integrated circuit according to the present invention will now be concretely described with reference to the accompanying drawings.

(First Embodiment)

A first embodiment adopts an SMT (Selective MT)-CMOS circuit system in which most of gate circuits in a semiconductor integrated circuit are constituted by transistors having a high threshold voltage and only some gate circuits are constituted by combining transistors having a high threshold voltage with transistors having a low threshold voltage, thereby increasing signal transmission rate and reducing consumption power. The gate circuit constituted by combining transistors having a high threshold voltage and transistors having a low threshold voltage will be referred to as an MT gate cell hereinafter.

FIG. 1 is a circuit diagram of the first embodiment of the semiconductor integrated circuit according to the present invention. In the circuit depicted in FIG. 1, only the gate circuit 1 on a critical path is constituted by combining transistors having a low threshold voltage with transistors having a high threshold voltage, and any other gate circuit 1 is constituted by transistors having a high threshold voltage.

In FIG. 1, the gate circuit 1 on the critical path is indicated by oblique lines. The gate circuit 1 indicated by the oblique lines is constituted by an MT gate cell constituted by a transistor having a high threshold voltage (second transistor) and a transistor having a low threshold voltage (first transistor). This MT gate cell may have the circuit structure similar to that in FIG. 9 or a later-described circuit structure.

Each switch circuit 10 for switching whether a power supply voltage is supplied to the MT gate cell is connected to a power supply line of the MT gate cell shown in FIG. 1. This switch circuit 10 is constituted by a PMOS transistor connected to a power supply voltage terminal VDD and an NMOS transistor connected to a ground voltage terminal. Moreover, a control circuit 2 for controlling the switch circuit 10 is provided in the circuit depicted in FIG. 1. The control circuit 2 in FIG. 1 controls ON/OFF of the PMOS transistor and the NMOS transistor within the

switch circuit 10 to switch whether the power supply voltage is supplied to the MT gate cell.

On the other hand, FIG. 2 is a conventional circuit diagram corresponding to the circuit depicted in FIG. 1. As apparent from FIGS. 1 and 2, the circuit shown in FIG. 1 is different from the circuit illustrated in FIG. 2 in that the MT gate cell substitutes for the gate circuit 1 on the critical path and that the control circuit 2 for switching whether the power is supplied to the MT gate cell is provided.

In case of FIG. 1 circuit, since the gate circuit 1 on the critical path is constituted by the MT gate cell, the signal transmission rate on the critical path can be increased. On the other hand, since any other circuit is constituted by a transistor having a high threshold voltage, the leak electric current can be suppressed in active state.

FIG. 3 is a circuit diagram showing a first concrete example of an MT gate cell constituting the gate circuit 1 of FIG. 1. The circuit of FIG. 3 includes an NAND circuit (gate circuit) 3 composed of transistors having a low threshold voltage, and a transistor (second transistor) Q1 for switching whether the power supply voltage is supplied to the NAND circuit 3. This transistor Q1 is a PMOS transistor having a high threshold voltage.

In case of the circuit illustrated in FIG. 3, when the transistor Q1 is turned on, the power supply voltage is supplied to the NAND circuit 3, and this NAND circuit 3 operates at a high speed. On the other hand, when the transistor Q1 is turned off, the leak path of the NAND circuit 3 is shut off, thereby reducing the leak electric current.

Since the circuit depicted in FIG. 3 has the NAND circuit 3 directly connected to a ground line VSS, the leak path can be assuredly shut off by turning off the transistor Q1 when the NAND circuit 3 is in the standby mode. As a result, the consumption power in the standby mode can be decreased.

On the other hand, FIG. 4 is a circuit diagram showing a second concrete example of the MT gate cell. The circuit shown in FIG. 4 includes: an NAND circuit (gate circuit) 3 connected

between a power supply line VDD and a virtual ground line VSS1, a transistor (second transistor) Q2 connected between the virtual ground line VSS1 and a ground line VSS, and a transistor (third transistor) Q3 connected between an output terminal of the NAND circuit 3 and the power supply line VDD.

The NAND circuit 3 is constituted by transistors having a low threshold voltage, and the transistors Q2 and Q3 are transistors having a high threshold voltage.

In case of the circuit shown in FIG. 4, when one of the transistors Q2 and Q3 is turned on, the other is turned off, and vice versa. When the transistor Q2 is turned on, the power supply voltage is supplied to the NAND circuit 3 and the NAND circuit 3 operates at a high speed. At this moment, since the transistor Q3 is in the OFF state, an output of the NAND circuit 3 is given from its output terminal. On the other hand, when the transistor Q2 is turned off, the leak path of the NAND circuit 3 is shut off, and the NAND circuit 3 enters the standby mode. At this time, the transistor Q3 is turned on and the output terminal is pulled up to the high level.

In case of the circuit illustrated in FIG. 4, the transistor Q3 is connected to the output terminal of the NAND circuit 3 so that the output logic of the NAND circuit does not become unstable in the standby mode. This prevents the intermediate potential from being propagated to the gate circuit 1 on the rear stage (not shown), and a passing electric current does not flow to the gate circuit 1 on the rear stage.

On the other hand, FIG. 5 is a circuit diagram showing a third concrete example of the MT gate cell. The circuit shown in FIG. 5 includes: an NAND circuit (gate circuit) 3 connected between a virtual power supply line VDD1 and a virtual ground line VSS1, a transistor (second transistor) Q1 connected between the virtual power supply line VDD1 and a power supply line VDD, a transistor (third transistor) Q2 connected between the virtual ground line VSS1 and a ground line VSS, and a data holding circuit (storage circuit) 4 connected to an output terminal of the NAND circuit 3.

The NAND circuit 3 is constituted by transistors having

a low threshold voltage, and the transistors Q1 and Q2 are transistors having a high threshold voltage.

The data holding circuit 4 has an inverter 5 connected to the output terminal of the NAND circuit 3, and a clocked inverter 6 connected between an output terminal of the inverter 5 and the output terminal of the NAND circuit 3. The clocked inverter 6 does not perform the data holding operation in the active mode when the transistors Q1 and Q2 are ON, but holds the output logic of the NAND circuit 3 in the standby mode when the transistors Q1 and Q2 are OFF.

In the circuit shown in FIG. 5, since the data is held in the data holding circuit 4 in the standby mode, a passing electric current does not flow to the gate circuit 1 on the rear stage as similar to the circuit in FIG. 4. In addition, since a signal is not propagated at the time of reactivation, the time required for reactivation is short and the consumption power used by reactivation is also small.

On the other hand, FIG. 6 is a circuit diagram showing a fourth concrete example of the MT gate cell. The circuit illustrated in FIG. 6 is similarly constituted as the circuit in FIG. 5 except that a bypass circuit 7 is provided instead of the data holding circuit.

The bypass circuit 7 in FIG. 6 has the same circuit structure as the NAND circuit 3, and is connected between a power supply line VDD and a ground line VSS and connected to the NAND circuit 3 in parallel. However, the NAND circuit 3 is constituted by transistors having a low threshold voltage, whereas the bypass circuit 7 is constituted by transistors having a high threshold voltage.

The NAND circuit 3 becomes active only when the transistors Q1 and Q2 are ON, whereas the bypass circuit 7 is constantly active.

When the transistors Q1 and Q2 are ON, the NAND circuit 3 and the bypass circuit 7 output signals having the same logic. On the other hand, when the transistors Q1 and Q2 are OFF, the NAND circuit 3 does not operate, but the bypass circuit 7 continuously operates, and hence the output logic of the circuit

in FIG. 6 does not become unstable. Thus, this prevents the intermediate potential from being propagated to the gate circuit 1 on the rear stage, and the passing electric current does not flow to the gate circuit 1 on the rear stage.

As described above, in the first embodiment, only some gate circuits 1 in the semiconductor integrated circuit (for example, the gate circuit 1 on the critical path) are constituted by the MT gate cells, and any other gate circuits 1 are constituted by transistors having a high threshold voltage. Therefore, only some gate circuits 1 can operate at a high speed, and the overall leak electric current can be suppressed, thereby reducing the consumption power.

Although examples in which the NAND circuit 3 is provided in the MT gate cell have been described with reference to FIGS. 3 to 6, any other gate circuit 1 than the NAND circuit 3 may be provided. However, this embodiment is characterized in that the transistors in the gate circuit having no intermediate node are constituted by transistors having a low threshold voltage.

For example, FIG. 7A shows an example of a gate circuit having no intermediate node and depicts a composite gate circuit obtained by combining an AND gate, an OR gate and an NAND gate. As shown in FIG. 7B in detail, the gate circuit shown in FIG. 7A is constituted by PMOS transistors Q4 to Q7 and NMOS transistors Q8 to Q11. Input signals A to D are inputted to respective gate terminals of the transistors Q4 to Q11. Each source/drain terminal of the transistors Q4 to Q11 is connected to a source/drain terminal of another transistor or an output terminal Z. That is, a number of stages that the input signals A to D pass through any gate terminal of the transistors Q4 to Q11 is only one.

Since the threshold voltage of the transistors constituting such a gate circuit having no intermediate node within the MT gate cell as shown in FIG. 7A is set lower than the threshold voltage of the transistors constituting other circuits, only this gate circuit can be driven at a high speed.

Incidentally, as the gate circuit having no intermediate node, various kinds of composite gate circuits such as shown in

FIG. 7A can be considered besides basic NAND circuits or NOR circuits.

(Second Embodiment)

A second embodiment constitutes some gate circuits 1 in a flip flop are constituted by MT gate cells.

FIG. 8 is a circuit diagram showing a second embodiment of a semiconductor integrated circuit according to the present invention. The semiconductor integrated circuit shown in FIG. 8 is a D flip flop, and this D flip flop is constituted by clocked inverters (first and second conduction interception circuits) 11 and 12 consisting of MT gate cells, inverters 13 to 15, and storage circuits (first and second storage circuits) 16 and 17 consisting of transistors having a high threshold value. The storage circuits 16 and 17 are constituted by the inverters and the clocked inverters as similar to the data holding circuit 4 shown in FIG. 5.

The storage circuits 16 and 17 in the flip flop are used for holding the output logic of the clocked inverter on a preceding stage and rarely affect the operation speed of the flip flop. Therefore, in this embodiment, the storage circuit is constituted by transistors having a high threshold value, thereby reducing the leak electric current.

On the other hand, the clocked inverters 11 and 12 and the inverters 13 to 15 in the flip flop are constituted by the MT gate cells as similar to FIGS. 3 to 6. Since the clocked inverters 11 and 12 and the inverters 13 to 15 function to transmit signals, the operation speed of the flip flop can be improved by constituting these inverters by the MT gate cells.

As described above, in the second embodiment, among a plurality of circuits constituting the flip flop, since only the clocked inverters 11 and 12 and the inverters 13 to 15 which affect the operation speed are formed by the MT gate cells and any other circuits are constituted by transistors having a high threshold voltage, the operation speed of the flip flop can be improved while the leak electric current can be reduced.

Incidentally, although an example in which the D flip flop is constituted has been described with reference to FIG. 8, the

present invention can be similarly applied to various kinds of flip flops other than the D flip flop. For example, although the inverters 13 to 15 are connected to the rear stage of the storage circuit 17, any circuit other than the inverters may be connected to the rear stage of the storage circuit 17.

Further, the circuit structure of the storage circuits 16 and 17 is not restricted to a specific type. For example, inverters may substitute for the clocked inverters in the storage circuits 16 and 17.